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REDUCING THE EFFECTS OF NOISE IN NON-VOLATILE MEMORIES THROUGH MULTIPLE READS

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RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 10/439,5[illegible] filed May 16, 2003, now U.S. Patent 6,785,164, which is a divisional of U.S. application Ser. No. 10/052,888, filed January 18, 2002, now U.S. Patent 6,621,739.

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates generally to computer readable memory devices, and, more specifically, to methods for reducing noise when reading their information content.

Background Information

[0002] In non-volatile semiconductor memories, such as EEPROMs, the amount of data stored per memory cell has been increased in order to increase storage densities. At the same time, the operating voltages of such devices have decreased to reduce power consumption. This results in a greater number states stored in a smaller range of voltage or current values. As the voltage or current separation between data states decreases, the effects of noise become more significant in the reading of these cells. For example, variations in the threshold value acceptable in a binary storage, 5 volts EEPROM cell may no longer be acceptable in a device operating at 3 volts with four or more bits storable per cell. Some consequences of noise, and methods for dealing with it, in a non-volatile memory are described in U.S. patent number 6,044,019, which is hereby incorporated by reference.

[0003] An example of noisy behaviour is shown in Figure 1A, which is adapted from patent number 6,044,019. This figure shows the variation in the current flowing through a memory cell in response to a particular set of bias conditions. The current fluctuates by an amount ΔI due to various noise effects in the memory cell and interfacing circuitry. If, for example, the memory circuit works by current sensing, as the separation between states approaches ΔI, the noise will begin to produce erroneous read values. Although the consequences of noise can be decreased by integration sensing techniques, such as those in patent number 6,044,019, or treated with error correction code (ECC) or other equivalent error management, such as is described in U.S. patent 5,418,752, which is

description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figures 1A-C show examples of noisy response in a memory cell.

[0009] Figure 2 illustrates the effect of noise on a program and verify operation.

[0010] Figure 3 is a schematic block diagram of the operation of the present invention according to an exemplary embodiment.

[0011] Figures 4A and 4B are block diagrams of circuit embodiments of some aspects of the present invention.

[0012] Figure 5 is a schematic representation of binary search implementation of an exemplary embodiment.

DESCRIPTION OF REPRESENTATIVE EMBODIMENTS

[0013] The storage capacity of non-volatile semiconductor memories has increased both by the reduction in the physical size of the individual components of the circuits including the memory cell and by increasing the amount of data storable in an individual memory cell. For example, devices such as those described in U.S. patents 5,712,180 and 6,103,573 and U.S. patent applications serial no. 09/505,555, filed on February 17, 2000, and serial no. 09/667,344, filed on September 22, 2000, which are all assigned to SanDisk Corporation and which are all hereby incorporated herein by this reference, can store four or more logical bits per physical floating gate storage transistor. In the case of four logical bits, this storage will require each floating gate to be able to have encoded within it one of sixteen possible memory states. Each one of these memory states corresponds to a unique value, or, more accurately, a narrow range of values, of stored charge on the floating gate which is sufficiently separated from its neighboring states' charge storage range of values to clearly differentiate it from those neighboring states as well as all the other states. This is true for both a normal read operation as well as for a verify read done